Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-26. Canceled

Claim 27-35. Canceled

Claim 36. (Currently amended) An integrated circuit comprising:

a pull-up MOS transistor having a source terminal coupled ~~between~~ to a first supply voltage and a drain terminal coupled to an input/output [[a]] pad;

a pull-down MOS transistor having a drain terminal coupled ~~between~~ to the input/output pad and a source terminal coupled to a second supply voltage that is lower than the first supply voltage;

a first MOS transistor ~~switch~~ having a source~~/drain~~ terminal coupled to the first supply voltage and a bulk terminal coupled to the bulk terminal of the pull-up MOS transistor;

an active diode having a first terminal coupled to the drain~~/source~~ terminal of the first MOS transistor ~~switch~~, and a second terminal coupled to the input/output pad; and

a biasing circuit coupled between the input/out pad and the first supply voltage and adapted to apply to bulk ~~regions~~ terminals of the pull-up MOS transistor and the first MOS transistor ~~switch~~ the higher of a voltage applied to the input/output pad and the first supply voltage.

Claim 37. (Currently amended) The integrated circuit of claim 36 further comprising:

an input buffer coupled directly to the input/output pad.

Claim 38. (Previously presented) The electronic circuit of claim 36 further comprising:

a first predriver circuit coupled to a gate terminal of the pull-up MOS transistor; and

a second predriver circuit coupled to a gate terminal of the pull-down MOS transistor.

Claim 39. (Currently amended) An integrated circuit comprising:

a pull-up MOS transistor having a source terminal coupled ~~between~~ to ~~a pad and~~ a first supply voltage and a drain terminal coupled to an input/output ;

a pull-down MOS transistor having a drain terminal coupled ~~between~~ to the input/output pad and a source terminal coupled to a second supply voltage that is lower than the first supply voltage;

a first MOS transistor ~~switch~~ having a source~~/drain~~ terminal coupled to the first supply voltage and a bulk terminal coupled to a bulk terminal of the pull-up MOS transistor;

a second MOS transistor ~~switch~~ having a drain terminal coupled ~~between the first MOS transistor switch and~~ to the input/output pad, a source terminal coupled to the drain terminal of the ~~second~~ first MOS transistor; and ~~switch having~~ a bulk terminal coupled to the bulk and drain terminals ~~terminal~~ of the first MOS transistor ~~switch and a common source/drain terminal of the first and second MOS transistor switches~~;

a comparator circuit coupled to the input/output pad and the first supply voltage, wherein the comparator circuit provides an output signal having a first state if a voltage on the input/output pad is higher than the first supply voltage, and a second state if the voltage on the input/output pad is lower than the first supply voltage; [[and]]

a first logic block configured to perform logical AND operation and being responsive to the output signal of the comparator circuit and an enable signal; and

a second logic block configured to perform logical inversion operation and being responsive to the first logic block, the second logic block being disposed between gate terminals of the first and the second MOS transistor switches.

Claim 40. (Previously presented) The electronic circuit of claim 39 further comprising:

a first predriver circuit coupled to a gate terminal of the pull-up MOS transistor; and

a second predriver circuit coupled to a gate terminal of the pull-down MOS transistor.

Claim 41. (Currently amended) An electronic system comprising:

an integrated circuit comprising:

a pull-up MOS transistor having a source terminal coupled ~~between~~ to a first supply voltage and a drain terminal coupled to an input/output pad;

a pull-down MOS transistor having a drain terminal coupled ~~between~~ to the input/output pad and a source terminal coupled to a second supply voltage that is lower than the first supply voltage;

a clamp MOS transistor having a source~~/drain~~ terminal coupled to the first supply voltage, a bulk terminal coupled to the bulk terminal of the pull-up MOS transistor, and a gate terminal receiving ~~coupled to~~ a control signal;

a diode having a first terminal coupled to the drain~~/source~~ terminal of the clamp MOS transistor, and a second terminal coupled to the input/output pad;

a biasing circuit coupled between the input/out pad and the first supply voltage and adapted to provide to the bulk terminals of the pull-up MOS transistor and the clamp MOS transistor the higher of a voltage ~~between a voltage on~~ applied to the input/output pad and the first supply voltage ~~to a well of the pull-up MOS transistor and the clamp MOS transistor~~; and

a resistor external to the integrated circuit.